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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/069,352	08/07/2002	Gilbert Wolrich	10559-308US1	7931
20985	7590	05/03/2007		
FISH & RICHARDSON, PC P.O. BOX 1022 MINNEAPOLIS, MN 55440-1022			EXAMINER HUISMAN, DAVID J	
			ART UNIT 2183	PAPER NUMBER
			MAIL DATE 05/03/2007	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/069,352	WOLRICH ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	David J. Huisman	2183	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 22 February 2007.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-38 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4, 6, 8, 9, 20-23, 25, 27 and 28 is/are rejected.
- 7) ☒ Claim(s) 5, 7, 10-19, 24, 26 and 29-38 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 June 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                       | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____                                      |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>2/22/2007</u> .   | 6) <input type="checkbox"/> Other: _____                          |

### **DETAILED ACTION**

1. Claims 1-38 have been examined.

#### ***Papers Submitted***

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: RCE, Amendment, IDS, and Power of Attorney as received on 2/22/2007

#### ***Information Disclosure Statement***

3. It is desirable to avoid the submission of long lists of documents if it can be avoided. Eliminate clearly irrelevant and marginally pertinent cumulative information. If a long list is submitted, highlight those documents which have been specifically brought to applicant's attention and/or are known to be of most significance. See *Penn Yan Boats, Inc. v. Sea Lark Boats, Inc.*, 359 F. Supp. 948, 175 USPQ 260 (S.D. Fla. 1972), *aff'd*, 479 F.2d 1338, 178 USPQ 577 (5<sup>th</sup> Cir. 1973), *cert. denied*, 414 U.S. 874 (1974). But cf. *Molins PLC v. Textron Inc.*, 48 F.3d 1172, 33 USPQ2d 1823 (Fed. Cir. 1995). See MPEP 2004.
4. An applicant's duty of disclosure of material and information is not satisfied by presenting a patent examiner with "a mountain of largely irrelevant [material] from which he is presumed to have been able, with his expertise and with adequate time, to have found the critical [material]. It ignores the real world conditions under which examiners work." *Rohm & Haas Co. v. Crystal Chemical Co.*, 722 F.2d 1556, 1573 [220 USPQ 289] (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984). (Emphasis in original). Patent applicant has a duty not just to disclose pertinent prior art references but to make a disclosure in such way as not to "bury" it

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within other disclosures of less relevant prior art; See *Golden Valley Microwave Foods Inc. v. Weaver Popcorn Co. Inc.*, 24 USPQ2d 1801 (N.D. Ind. 1992); *Molins PLC v. Textron Inc.*, 26 USPQ2d 1889, at 1899 (D.Del 1992); *Penn Yan Boats, Inc. v. Sea Lark Boats, Inc. et al.*, 175 USPQ 260, at 272 (S.D. Fl. 1972).

5. It is impractical for the examiner to thoroughly review each reference, given the number of references cited. By initialing each of the cited references on the accompanying 1449 forms, the examiner is merely acknowledging the submission of the cited references and merely indicating that only a cursory review was made of the cited references.

#### ***Withdrawn Rejections***

6. Applicant's arguments filed on February 22, 2007, with respect to Barry et al., U.S. Patent No. 6,446,190, have been fully considered and are persuasive. Therefore, the rejections associated with Barry have been withdrawn.

#### ***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 1-4, 6, 8-9, 20-23, 25, and 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Velingker, U.S. Patent No. 6,279,066.

9. Referring to claim 1, Velingker has taught a method of operating a processor comprising:

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a) receiving data specified by execution of a fast-write instruction in a processing stream

identified by a processing stream number. See Figs.2-4 and column 5, lines 19-50. Note from Fig.3 that multiple processors each execute different streams of instructions (threads 1, 2, and 3). When a stream wants access to a shared resource, it issues an instruction (fast-write instruction) to set a bit in the RNC (register).

b) the fast-write instruction further specifying a register, the register having multiple groups of bits, each group of bits associated with one of multiple streams available on the processor. See Figs.2-3, column 5, lines 19-50, and column 6, lines 10-18. In one embodiment of the invention, the resource negotiation cell (RNC) is a register with three groups of bits, each group comprising two bits (a request bit and a completion bit). Each group is associated with a different stream. When a stream wants to request a resource or indicate access completion, a fast-write instruction including data is issued to set an appropriate bit in the corresponding group.

c) selecting a group of bits associated with the processing stream, the group of bits being selected from the multiple groups of bits of the register specified by the fast-write instruction according to the processing stream number. Again, see column 5, lines 19-50, column 6, lines 10-18, and Figs.2-3. When a stream wants to access a shared resource or indicate access completion, the stream's group of bits is selected for modification.

d) loading the data into the selected bit positions of the register. See column 5, lines 19-50, column 6, lines 10-18, and Figs.2-3. When the stream wants to access a shared resource, it will write a '1' into a bit of the group of bits. And, when it is finished accessing the resource, it will write a '1' into another bit of the group of bits.

e) while Velingker has not explicitly taught that each stream executed by the processors in the multiprocessor system constitutes a thread, Official Notice is taken that in a multiprocessor system, each processor may be configured to execute a different thread. Further known are the advantages of multithreading. One such advantage is that one when thread is stalled, another thread may continue executing, as they are independent streams. With only a single thread, if the thread stalls, all resources stall. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Velingker's streams to be threads such that each processor executes a different thread.

10. Referring to claim 2, Velingker has taught a method as described in claim 1. Velingker has further taught that the register is a control and status register (CSR). See Fig.3. The register written to controls (and specifies the status of) shared resource access.

11. Referring to claim 3, Velingker has taught a method as described in claim 2. Velingker has not explicitly taught that the control and status register is coupled to a 64-bit wide first-in first-out (FIFO) bus. However, as shown in *In re Rose*, 105 USPQ 237 (CCPA 1955), changes in size are generally not given patentable weight or would have been an obvious improvement. Specifically, the size of Velingker's bus is not disclosed, but a 64-bit bus is a common bus size, which allows for more data to be transported at once than on a 32-bit bus or 16-bit bus, for instance. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Velingker's bus to be 64-bits wide. Furthermore, the bus is inherently FIFO because data that is sent over the bus at time A will arrive at its destination before data that is sent over the bus at time B (where  $B > A$ ).

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12. Referring to claim 4, Velingker has taught a method as described in claim 3.

Furthermore, it is deemed inherent in Velingker that the FIFO bus interfaces with Media Access Controller (MAC) devices. There must be devices which control the means for communicating across a bus. These devices are media access controllers as they control media access.

13. Referring to claim 6, Velingker has taught a method as described in claim 1. Velingker has further taught that the processing thread represents processing in a micro engine of a multithreaded processor. See Fig.1, and note that each processor (micro engine) processes a thread.

14. Referring to claim 8, Velingker has taught a method as described in claim 1. Velingker has further taught that the fast-write instruction comprises a token. See column 5, lines 19-50, and note that an instruction having a form equivalent to "WRITE REQUEST 1" will be issued. This instruction will write a '1' to the access bit. The '1' is the token.

15. Referring to claim 9, Velingker has taught a method as described in claim 8. Velingker has further taught that the token represents overriding qualifiers. Since the instruction writes to a register bit using the data provided in the instruction, the bit of the data (token) represents an overriding qualifier as the "old" bit of the selected group in the register will be overridden by the "new" data.

16. Referring to claims 20-21, 25, and 27-28, claims 20-21, 25, and 27-28 are rejected for the same reasons set forth in the rejection of claims 1-2, 6, and 8-9, respectively, because Velingker has taught instructions stored on a medium for performing the method of claims 1-2, 6, and 8-9.

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17. Referring to claims 22-23, claims 22-23 are rejected for the same reasons set forth in the rejection of claims 3-4, respectively, because Velingker has taught instructions stored on a medium for performing the method of claims 3-4.

***Allowable Subject Matter***

18. Claims 5, 7, 10-19, 24, 26, and 29-38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Response to Arguments***

19. Applicant's arguments filed on February 22, 2007, have been fully considered but they are not persuasive.

20. Applicant argues the novelty/rejection of claim 1 on page 14 of the remarks by stating that the bits set in Velingker are not arranged in a register. This argument is not found persuasive because the abstract discloses such a register (RNR).

21. Applicant argues the novelty/rejection of claim 1 on page 15 of the remarks by stating that the bits of the SRN are hardwired and that they are not loaded by any type of instruction. This argument is not found persuasive because (a) the examiner has found no reference of any hardwiring of bits in Velingker, and (b) if the bits were hardwired, then they could only have one value, as is known in the art, i.e., they wouldn't be settable or clearable, which is clearly not the case in Velingker, as the processor writes to and clears these bits. See the description of Fig.4.



***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DJH  
David J. Huisman  
April 16, 2007

